

In the claims:

Please amend the claims as follows:

Claims 1-10 (canceled).

11. (currently amended) A passenger transit car comprising:

- Σ 2
- a) at least one car drive motor;
 - b) at least one ~~a first plurality of~~ solenoids;
 - c) at least one ~~a second plurality of~~ mechanical switches;
 - 5 d) at least one ~~a third plurality of~~ motors for moving doors on said passenger transit car;
 - e) an electrical control unit comprising:

i) a mother board located in said control unit having at least one ~~a fourth plurality of~~ daughter boards wherein said
10 electrical control unit is connected to said at least one ~~first plurality of~~ solenoids, to said at least one ~~second plurality of~~ mechanical switches, and to said at least one ~~third plurality of~~ motors for moving doors on said passenger transit car;

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ii) a self-locking memory circuit located in said
15 control unit for a tristate ~~tri-state~~ data bus having multiple
1-8 bit lines, said self-locking memory circuit comprising:

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A) a non-clocked, non-inverting amplifier chip for connection to one of said bit lines;

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B) a resistor having a predetermined electrical
20 resistance connected across said non-clocked, non-inverting
amplifier chip; and

Σ2

C) wherein said self-locking memory circuit has
upper and lower voltage thresholds that cause said self-locking
memory circuit to change states when a level of voltage applied
25 to said self-locking memory circuit passes through one of said
thresholds.

12. (previously added) A passenger transit car according
to claim 11 wherein said passenger transit car ~~self-locking~~
~~memory circuit~~ includes:

a central processing unit;

(DSP)

5 a Digital Signal Processor_A for transceiving discrete
electrical inputs; and

a tri state data bus electrically connecting said Digital
Signal Processor to said central processing unit, said Digital
Signal Processor and said central processing unit having
10 different clock rates for accessing said tristate ~~tri-state~~ data
bus.

13. (previously added) A passenger transit car according
to claim 12 ~~11~~ wherein said passenger transit car ~~self-locking~~
~~memory circuit~~ includes:

(CPLD)

a Complex Programmable Logic Device[^] for transceiving
5 discrete electrical signals; and

wherein said tri state data bus electrically interconnects
said central processing unit, said Digital Signal Processor, and
said Complex Programmable Logic Device, said Digital Signal
Processor and said Complex Programmable Logic Device having clock
10 rates for accessing said tristate ~~tri-state~~ data bus that are
different from a clock rate at which said central processing unit
accesses said tri state data bus.

Claim 14 (canceled).
